AiP74LVC/LVCH8T245
8-bit Dual Supply Translating Transceiver; 3-state

Product Specification

Specification Revision History:

Version	Date	Description
2017-12-A1	2017-12	New
2023-04-B1	2023-04	Update the template

Contents

1、General Description

The AiP74LVC/LVCH8T245 are 8-bit dual supply translating transceivers with 3-state outputs that enable bidirectional level translation. They feature two data input-output ports (pins An and Bn), a direction control input (DIR), an output enable input ($\overline{OE}$) and dual supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). Both $V_{CC(A)}$ and $V_{CC(B)}$ can be supplied at any voltage between 1.2V and 5.5V making the device suitable for translating between any of the low voltage nodes (1.2V, 1.5V, 1.8V, 2.5V, 3.3V and 5.0V). Pins An, $\overline{OE}$ and DIR are referenced to $V_{CC(A)}$ and pins Bn are referenced to $V_{CC(B)}$. A HIGH on DIR allows transmission from An to Bn and a LOW on DIR allows transmission from Bn to An. The output enable input ($\overline{OE}$) can be used to disable the outputs so the buses are effectively isolated.

The devices are fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either $V_{CC(A)}$ or $V_{CC(B)}$ are at GND level, both A port and B port are in the high-impedance OFF-state.

Active bus hold circuitry in the AiP74LVCH8T245 holds unused or floating data inputs at a valid logic level.

Features:

- Wide supply voltage range:
  $V_{CC(A)}$: 1.2V to 5.5V
  $V_{CC(B)}$: 1.2V to 5.5V
- Maximum data rates:
  420Mbps (3.3V to 5.0V translation)
  210Mbps (translate to 3.3V)
  140Mbps (translate to 2.5V)
  75Mbps (translate to 1.8V)
  60Mbps (translate to 1.5V)
- Suspend mode
- ±24mA output drive (V_{CC}=3.0V)
- Inputs accept voltages up to 5.5V
- Low power consumption: 30uA maximum I_{CC}
- I_{OFF} circuitry provides partial Power-down mode operation
- Specified from -40℃ to +125℃
- Packaging information: TSSOP24/DHVQFN24

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP74LVC8T245 TA24.TB	TSSOP24	74LVC8T245	62 PCS/tube	200 tube/box	12400 PCS/box	Dimensions of plastic enclosure: 7.8mm×4.4mm Pin spacing: 0.65mm
AiP74LVCH8T245 TA24.TB	TSSOP24	74LVCH8T245	62 PCS/tube	200 tube/box	12400 PCS/box	Dimensions of plastic enclosure: 7.8mm×4.4mm Pin spacing: 0.65mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP74LVC8T245QE24.TR	DHVQFN24	74LVC8T245	3000 PCS/reel	3000 PCS/box	Dimensions of plastic enclosure: 5.5mm×3.5mm Pin spacing: 0.5mm
AiP74LVCH8T245QE24.TR	DHVQFN24	74LVCH8T245	3000 PCS/reel	3000 PCS/box	Dimensions of plastic enclosure: 5.5mm×3.5mm Pin spacing: 0.5mm
AiP74LVC8T245TA24.TR	TSSOP24	74LVC8T245	2500 PCS/reel	5000 PCS/box	Dimensions of plastic enclosure: 7.8mm×4.4mm Pin spacing: 0.65mm
AiP74LVCH8T245TA24.TR	TSSOP24	74LVCH8T245	2500 PCS/reel	5000 PCS/box	Dimensions of plastic enclosure: 7.8mm×4.4mm Pin spacing: 0.65mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram

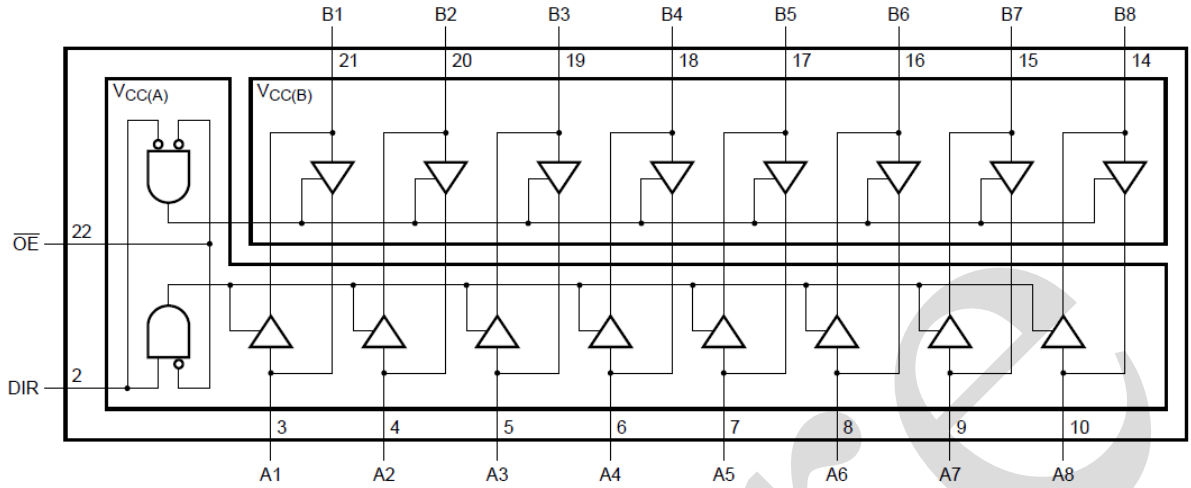


Figure 1. Logic symbol

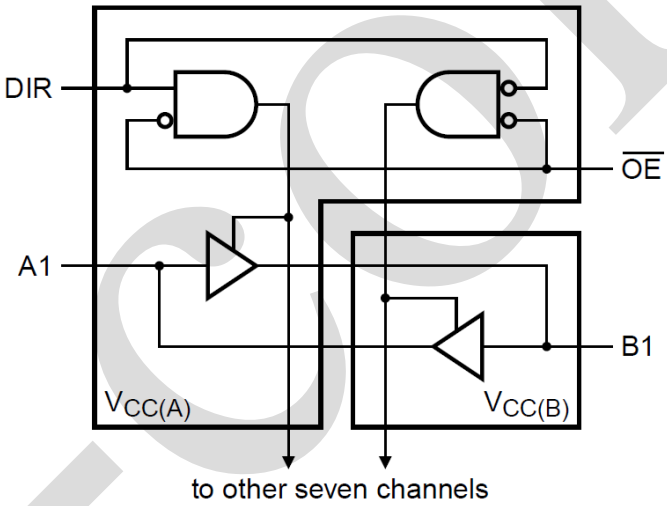
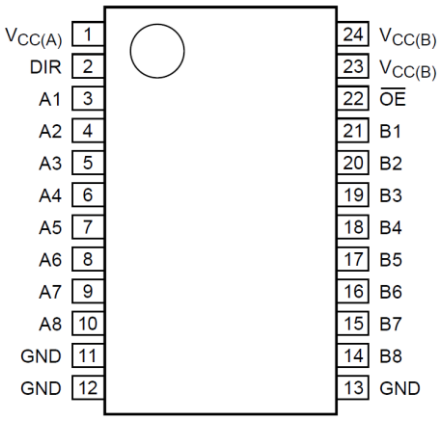
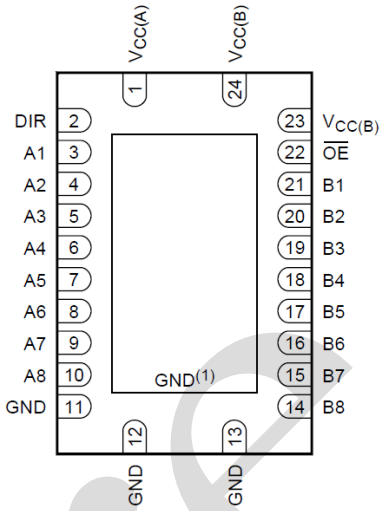


Figure 2. Logic diagram (one channel)

2.2、Pin Configurations



TSSOP24



DHVQFN24

Note:

(1) This is not a supply pin, the substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad however if it is soldered the solder land should remain floating or be connected to GND.

2.3、Pin Description

Pin No.	Pin Name	Description
1	$V_{CC(A)}$	supply voltage A (An inputs/outputs, $\overline{OE}$ and DIR inputs are referenced to $V_{CC(A)}$)
2	DIR	direction control
3,4,5,6,7,8,9,10	A1 to A8	data input or output
11	GND[1]	ground (0V)
12	GND[1]	ground (0V)
13	GND[1]	ground (0V)
21,20,19,18,17,16,15,14	B1 to B8	data input or output
22	$\overline{OE}$	output enable input (active LOW)
23	$V_{CC(B)}$	supply voltage B (Bn inputs/outputs are referenced to $V_{CC(B)}$)
24	$V_{CC(B)}$	supply voltage B (Bn inputs/outputs are referenced to $V_{CC(B)}$)

Note:[1]All GND pins must be connected to ground (0V).

2.4、Function Table

Supply voltage	Input		Input/output	
$V_{CC(A)}$, $V_{CC(B)}$	$\overline{OE}$	DIR	An	Bn
1.2V to 5.5V	L	L	An=Bn	input
1.2V to 5.5V	L	H	input	Bn=An
1.2V to 5.5V	H	X	Z	Z
GND	X	X	Z	Z

Note:

[1] H=HIGH voltage level; L=LOW voltage level; X=don't care; Z=high-impedance OFF-state.

[2] The An inputs/outputs, DIR and $\overline{OE}$ input circuit is referenced to $V_{CC(A)}$; The Bn inputs/outputs circuit
is referenced to $V_{CC(B)}$.

[3] If at least one of $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into suspend mode.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage A	$V_{CC(A)}$	-	-0.5	+6.5	V
supply voltage B	$V_{CC(B)}$	-	-0.5	+6.5	V
input clamping current	I_{IK}	V_I<0V	-50	-	mA
input voltage	V_I	-[1]	-0.5	+6.5	V
output clamping current	I_{OK}	V_O<0V	-50	-	mA
output voltage	V_O	Active mode[1][2][3]	-0.5	V_{CCO}+0.5	V
		Suspend or 3-state mode[1]	-0.5	+6.5	V
output current	I_O	V_O=0V to V_{CCO}[2]	-	±50	mA
supply current	I_{CC}	$I_{CC(A)}$ or $I_{CC(B)}$; per V_{CC} pin	-	100	mA
ground current	I_{GND}	per GND pin	-100	-	mA
storage temperature	T_{stg}	-	-65	+150	℃
total power dissipation	P_{tot}	-	-	500	mW
Soldering temperature	T_L	10s	260		℃

Note:

[1] The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] V_{CCO} is the supply voltage associated with the output port.

[3] V_{CCO}+0.5V should not exceed 6.5V.

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage A	$V_{CC(A)}$	-	1.2	-	5.5	V
supply voltage B	$V_{CC(B)}$	-	1.2	-	5.5	V
input voltage	V_I	-	0	-	5.5	V
output voltage	V_O	Active mode[1]	0	-	V_{CCO}	V
		Suspend or 3-state mode	0	-	5.5	V
ambient temperature	T_{amb}	-	-40	-	+125	℃
input transition rise and fall rate	Δt/ΔV	V_{CCI}=1.2V[2]	-	-	20	ns/V
		V_{CCI}=1.4V to 1.95V	-	-	20	ns/V
		V_{CCI}=2.3V to 2.7V	-	-	20	ns/V
		V_{CCI}=3.0V to 3.6V	-	-	10	ns/V
		V_{CCI}=4.5V to 5.5V	-	-	5	ns/V

Note:

[1] V_{CCO} is the supply voltage associated with the output port.

[2] V_{CCI} is the supply voltage associated with the input port.

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(T_{amb}=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level output voltage	V_{OH}	V_I=V_{IH} or V_{IL} [1]	I_O=-3mA; V_{CCO}=1.2V	-	1.09	-	V
LOW-level output voltage	V_{OL}	V_I=V_{IH} or V_{IL}	I_O=3mA; V_{CCO}=1.2V[1]	-	0.07	-	V
input leakage current	I_I	DIR, $\overline{OE}$ input; V_I=0V to 5.5V; V_{CCI}=1.2V to 5.5V[2]		-	-	±1	uA
bus hold LOW current	I_{BHL}	A or B port; V_I=0.42V; V_{CCI}=1.2V[2]		-	19	-	uA
bus hold HIGH current	I_{BHH}	A or B port; V_I=0.78V; V_{CCI}=1.2V[2]		-	-19	-	uA
bus hold LOW overdrive current	I_{BHLO}	A or B port; V_{CCI}=1.2V[2][3]		-	19	-	uA
bus hold HIGH overdrive current	I_{BHHO}	A or B port; V_{CCI}=1.2V[2][3]		-	-19	-	uA
OFF-state output current	I_{OZ}	A or B port; V_O=0V or V_{CCO}; V_{CCO}=1.2V to 5.5V[1]		-	-	±1	uA
		suspend mode A port; V_O=0Vor V_{CCO}; $V_{CC(A)}$=5.5V; $V_{CC(B)}$=0V[1]		-	-	±1	uA
		suspend mode B port; V_O=0Vor V_{CCO}; $V_{CC(A)}$=0V; $V_{CC(B)}$=5.5V[1]		-	-	±1	uA
power-off leakage current	I_{OFF}	A port; V_I or V_O=0V to 5.5V; $V_{CC(A)}$=0V; $V_{CC(B)}$=1.2V to 5.5V		-	-	±1	uA
		B port; V_I or V_O=0V to 5.5V; $V_{CC(B)}$=0V; $V_{CC(A)}$=1.2V to 5.5V		-	-	±1	uA

input capacitance	C_I	DIR, $\overline{OE}$ input; V_I=0V or 3.3V; $V_{CC(A)}$=3.3V	-	3	-	pF
input/output capacitance	$C_{I/O}$	A and B port; V_O=3.3V or 0V; $V_{CC(A)}$ =$V_{CC(B)}$=3.3V	-	6.5	-	pF

Note:

[1] V_{CCO} is the supply voltage associated with the output port.

[2] V_{CCI} is the supply voltage associated with the data input port.

[3] To guarantee the node switches, an external driver must source/sink at least I_{BHLO}/I_{BHHO} when the input is in the range V_{IL} to V_{IH}.

3.3.2、DC Characteristics 2

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	data input[1]	V_{CCI}=1.2V	0.8V_{CCI}	-	-	V
			V_{CCI}=1.4V to 1.95V	0.65V_{CCI}	-	-	V
			V_{CCI}=2.3V to 2.7V	1.7	-	-	V
			V_{CCI}=3.0V to 3.6V	2.0	-	-	V
			V_{CCI}=4.5V to 5.5V	0.7V_{CCI}	-	-	V
		DIR, $\overline{OE}$ input	V_{CCI}=1.2V	0.8$V_{CC(A)}$	-	-	V
			V_{CCI}=1.4V to 1.95V	0.65$V_{CC(A)}$	-	-	V
			V_{CCI}=2.3V to 2.7V	1.7	-	-	V
			V_{CCI}=3.0V to 3.6V	2.0	-	-	V
			V_{CCI}=4.5V to 5.5V	0.7$V_{CC(A)}$	-	-	V
LOW-level input voltage	V_{IL}	data input[1]	V_{CCI}=1.2V	-	-	0.2V_{CCI}	V
			V_{CCI}=1.4V to 1.95V	-	-	0.35V_{CCI}	V
			V_{CCI}=2.3V to 2.7V	-	-	0.7	V
			V_{CCI}=3.0V to 3.6V	-	-	0.8	V
			V_{CCI}=4.5V to 5.5V	-	-	0.3V_{CCI}	V
		DIR, $\overline{OE}$ input	V_{CCI}=1.2V	-	-	0.2$V_{CC(A)}$	V
			V_{CCI}=1.4V to 1.95V	-	-	0.35$V_{CC(A)}$	V
			V_{CCI}=2.3V to 2.7V	-	-	0.7	V
			V_{CCI}=3.0V to 3.6V	-	-	0.8	V
			V_{CCI}=4.5V to 5.5V	-	-	0.3$V_{CC(A)}$	V
HIGH-level output voltage	V_{OH}	V_I=V_{IH}	I_O=-100uA; V_{CCO}=1.2V to 4.5V[2]	V_{CCO}-0.1	-	-	V
			I_O=-6mA; V_{CCO}=1.4V	1.0	-	-	V
			I_O=-8mA; V_{CCO}=1.65V	1.2	-	-	V
			I_O=-12mA; V_{CCO}=2.3V	1.9	-	-	V
			I_O=-24mA; V_{CCO}=3.0V	2.4	-	-	V
			I_O=-32mA; V_{CCO}=4.5V	3.8	-	-	V
LOW-level output voltage	V_{OL}	V_I=V_{IL}[2]	I_O=100uA; V_{CCO}=1.2V to 4.5V	-	-	0.1	V
			I_O=6mA; V_{CCO}=1.4V	-	-	0.3	V
			I_O=8mA; V_{CCO}=1.65V	-	-	0.45	V
			I_O=12mA; V_{CCO}=2.3V	-	-	0.3	V
			I_O=24mA; V_{CCO}=3.0V	-	-	0.55	V

			I_O=32mA; V_{CCO}=4.5V	-	-	0.55	V
input leakage current	I_I	DIR, $\overline{OE}$ input;V_I=0V or 5.5V; V_{CCI}=1.2V to 5.5V		-	-	±2	uA
bus hold LOW current	I_{BHL}	A or B port[1]	V_I=0.49V; V_{CCI}=1.4V	15	-	-	uA
			V_I=0.58V; V_{CCI}=1.65V	25	-	-	uA
			V_I=0.70V; V_{CCI}=2.3V	45	-	-	uA
			V_I=0.80V; V_{CCI}=3.0V	100	-	-	uA
			V_I=1.35V; V_{CCI}=4.5V	100	-	-	uA
bus hold HIGH current	I_{BHH}	A or B port[1]	V_I=0.91V; V_{CCI}=1.4V	-15	-	-	uA
			V_I=1.07V; V_{CCI}=1.65V	-25	-	-	uA
			V_I=1.70V; V_{CCI}=2.3V	-45	-	-	uA
			V_I=2.00V; V_{CCI}=3.0V	-100	-	-	uA
			V_I=3.15V; V_{CCI}=4.5V	-100	-	-	uA
bus hold LOW overdrive current	I_{BHLO}	A or B port[1][3]	V_{CCI}=1.6V	125	-	-	uA
			V_{CCI}=1.95V	200	-	-	uA
			V_{CCI}=2.7V	300	-	-	uA
			V_{CCI}=3.6V	500	-	-	uA
			V_{CCI}=5.5V	900	-	-	uA
bus hold HIGH overdrive current	I_{BHHO}	A or B port[1][3]	V_{CCI}=1.6V	-125	-	-	uA
			V_{CCI}=1.95V	-200	-	-	uA
			V_{CCI}=2.7V	-300	-	-	uA
			V_{CCI}=3.6V	-500	-	-	uA
			V_{CCI}=5.5V	-900	-	-	uA
OFF-state output current	I_{OZ}	A or B port; V_O=0V or V_{CCO}; V_{CCO}=1.2V to 5.5V[2]		-	-	±2	uA
		suspend mode A port; V_O=0V or V_{CCO}; $V_{CC(A)}$=5.5V; $V_{CC(B)}$=0V[2]		-	-	±2	uA
		suspend mode B port; V_O=0V or V_{CCO}; $V_{CC(A)}$=0V; $V_{CC(B)}$=5.5V[2]		-	-	±2	uA
power-off leakage current	I_{OFF}	A port; V_I or V_O=0V to 5.5V; $V_{CC(A)}$=0V; $V_{CC(B)}$=1.2V to 5.5V		-	-	±2	uA
		B port; V_I or V_O=0V to 5.5V; $V_{CC(B)}$=0V; $V_{CC(A)}$=1.2V to 5.5V		-	-	±2	uA
supply current	I_{CC}	A port; V_I=0V or V_{CCI}; I_O=0A[1]	$V_{CC(A)}$,$V_{CC(B)}$=1.2V to 5.5V	-	-	15	uA
			$V_{CC(A)}$=5.5V;$V_{CC(B)}$=0V	-	-	15	uA
			$V_{CC(A)}$=0V;$V_{CC(B)}$=5.5V	-2	-	-	uA
		B port; V_I=0V or V_{CCI}; I_O=0A	$V_{CC(A)}$,$V_{CC(B)}$=1.2V to 5.5V	-	-	15	uA
			$V_{CC(B)}$=0V;$V_{CC(A)}$=5.5V	-2	-	-	uA
			$V_{CC(B)}$=5.5V;$V_{CC(A)}$=0V	-	-	15	uA
		A plus B port ($I_{CC(A)}$+$I_{CC(B)}$); I_O=0A;	$V_{CC(A)}$,$V_{CC(B)}$=1.2V to 5.5V	-	-	25	uA

		V_I=0V or V_{CCI}					
additional supply current	ΔI_{CC}	per input; $V_{CC(A)}$,$V_{CC(B)}$ =3.0V to 5.5V	DIR and $\overline{OE}$ input; DIR or $\overline{OE}$ input at $V_{CC(A)}$-0.6V; A port at $V_{CC(A)}$ or GND; B port=open	-	-	50	uA
			A port; A port at $V_{CC(A)}$-0.6V; DIR at $V_{CC(A)}$; B port=open[4]	-	-	50	uA
			B port; B port at $V_{CC(B)}$-0.6V; DIR at GND; A port=open[4]	-	-	50	uA

Note:

[1] V_{CCI} is the supply voltage associated with the data input port.

[2] V_{CCO} is the supply voltage associated with the output port.

[3] To guarantee the node switches, an external driver must source/sink at least I_{BHLO}/I_{BHHO} when the input is in the range V_{IL} to V_{IH}.

[4] For non bus hold parts only (AiP74LVC8T245).

3.3.3、DC Characteristics 3

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	data input[1]	V_{CCI}=1.2V	0.8V_{CCI}	-	-	V
			V_{CCI}=1.4V to 1.95V	0.65V_{CCI}	-	-	V
			V_{CCI}=2.3V to 2.7V	1.7	-	-	V
			V_{CCI}=3.0V to 3.6V	2.0	-	-	V
			V_{CCI}=4.5V to 5.5V	0.7V_{CCI}	-	-	V
		DIR, $\overline{OE}$ input	V_{CCI}=1.2V	0.8$V_{CC(A)}$	-	-	V
			V_{CCI}=1.4V to 1.95V	0.65$V_{CC(A)}$	-	-	V
			V_{CCI}=2.3V to 2.7V	1.7	-	-	V
			V_{CCI}=3.0V to 3.6V	2.0	-	-	V
			V_{CCI}=4.5V to 5.5V	0.7$V_{CC(A)}$	-	-	V
LOW-level input voltage	V_{IL}	data input[1]	V_{CCI}=1.2V	-	-	0.2V_{CCI}	V
			V_{CCI}=1.4V to 1.95V	-	-	0.35V_{CCI}	V
			V_{CCI}=2.3V to 2.7V	-	-	0.7	V
			V_{CCI}=3.0V to 3.6V	-	-	0.8	V
			V_{CCI}=4.5V to 5.5V	-	-	0.3V_{CCI}	V
		DIR, $\overline{OE}$ input	V_{CCI}=1.2V	-	-	0.2$V_{CC(A)}$	V
			V_{CCI}=1.4V to 1.95V	-	-	0.35$V_{CC(A)}$	V
			V_{CCI}=2.3V to 2.7V	-	-	0.7	V
			V_{CCI}=3.0V to 3.6V	-	-	0.8	V
			V_{CCI}=4.5V to 5.5V	-	-	0.3$V_{CC(A)}$	V
HIGH-level	V_{OH}	V_I=V_{IH}	I_O=-100uA;	V_{CCO}-0.1	-	-	V

output voltage			V_{CCO}=1.2V to 4.5V[2]				
			I_O=-6mA; V_{CCO}=1.4V	1.0	-	-	V
			I_O=-8mA; V_{CCO}=1.65V	1.2	-	-	V
			I_O=-12mA; V_{CCO}=2.3V	1.9	-	-	V
			I_O=-24mA; V_{CCO}=3.0V	2.4	-	-	V
			I_O=-32mA; V_{CCO}=4.5V	3.8	-	-	V
LOW-level output voltage	V_{OL}	V_I=V_{IL}[2]	I_O=100uA; V_{CCO}=1.2V to 4.5V	-	-	0.1	V
			I_O=6mA; V_{CCO}=1.4V	-	-	0.3	V
			I_O=8mA; V_{CCO}=1.65V	-	-	0.45	V
			I_O=12mA; V_{CCO}=2.3V	-	-	0.3	V
			I_O=24mA; V_{CCO}=3.0V	-	-	0.55	V
			I_O=32mA; V_{CCO}=4.5V	-	-	0.55	V
input leakage current	I_I	DIR, $\overline{OE}$ input;V_I=0V or 5.5V; V_{CCI}=1.2V to 5.5V		-	-	±10	uA
bus hold LOW current	I_{BHL}	A or B port[1]	V_I=0.49V; V_{CCI}=1.4V	10	-	-	uA
			V_I=0.58V; V_{CCI}=1.65V	20	-	-	uA
			V_I=0.70V; V_{CCI}=2.3V	45	-	-	uA
			V_I=0.80V; V_{CCI}=3.0V	80	-	-	uA
			V_I=1.35V; V_{CCI}=4.5V	100	-	-	uA
bus hold HIGH current	I_{BHH}	A or B port[1]	V_I=0.91V; V_{CCI}=1.4V	-10	-	-	uA
			V_I=1.07V; V_{CCI}=1.65V	-20	-	-	uA
			V_I=1.70V; V_{CCI}=2.3V	-45	-	-	uA
			V_I=2.00V; V_{CCI}=3.0V	-80	-	-	uA
			V_I=3.15V; V_{CCI}=4.5V	-100	-	-	uA
bus hold LOW overdrive current	I_{BHLO}	A or B port[1][3]	V_{CCI}=1.6V	125	-	-	uA
			V_{CCI}=1.95V	200	-	-	uA
			V_{CCI}=2.7V	300	-	-	uA
			V_{CCI}=3.6V	500	-	-	uA
			V_{CCI}=5.5V	900	-	-	uA
bus hold HIGH overdrive current	I_{BHHO}	A or B port[1][3]	V_{CCI}=1.6V	-125	-	-	uA
			V_{CCI}=1.95V	-200	-	-	uA
			V_{CCI}=2.7V	-300	-	-	uA
			V_{CCI}=3.6V	-500	-	-	uA
			V_{CCI}=5.5V	-900	-	-	uA
OFF-state output current	I_{OZ}	A or B port; V_O=0V or V_{CCO}; V_{CCO}=1.2V to 5.5V[2]		-	-	±10	uA
		suspend mode A port; V_O=0V or V_{CCO}; $V_{CC(A)}$=5.5V; $V_{CC(B)}$=0V[2]		-	-	±10	uA
		suspend mode B port; V_O=0V or V_{CCO}; $V_{CC(A)}$=0V; $V_{CC(B)}$=5.5V[2]		-	-	±10	uA
power-off leakage current	I_{OFF}	A port; V_I or V_O=0V to 5.5V; $V_{CC(A)}$=0V; $V_{CC(B)}$=1.2V to 5.5V		-	-	±10	uA
		B port; V_I or V_O=0V to 5.5V;		-	-	±10	uA

		$V_{CC(B)}$=0V; $V_{CC(A)}$=1.2V to 5.5V					
supply current	I_{CC}	A port; V_I=0V or V_{CCI}; I_O=0A[1]	$V_{CC(A)}$,$V_{CC(B)}$=1.2V to 5.5V	-	-	20	uA
			$V_{CC(A)}$=5.5V;$V_{CC(B)}$=0V	-	-	20	uA
			$V_{CC(A)}$=0V;$V_{CC(B)}$=5.5V	-4	-	-	uA
		B port; V_I=0V or V_{CCI}; I_O=0A	$V_{CC(A)}$,$V_{CC(B)}$=1.2V to 5.5V	-	-	20	uA
			$V_{CC(B)}$=0V;$V_{CC(A)}$=5.5V	-4	-	-	uA
			$V_{CC(B)}$=5.5V;$V_{CC(A)}$=0V	-	-	20	uA
		A plus B port ($I_{CC(A)}$+$I_{CC(B)}$); I_O=0A; V_I=0V or V_{CCI}	$V_{CC(A)}$,$V_{CC(B)}$=1.2V to 5.5V	-	-	30	uA
additional supply current	ΔI_{CC}	per input; $V_{CC(A)}$,$V_{CC(B)}$ =3.0V to 5.5V	DIR and $\overline{OE}$ input; DIR or $\overline{OE}$ input at $V_{CC(A)}$-0.6V; A port at $V_{CC(A)}$ or GND; B port=open	-	-	75	uA
			A port; A port at $V_{CC(A)}$-0.6V; DIR at $V_{CC(A)}$; B port=open[4]	-	-	75	uA
			B port; B port at $V_{CC(B)}$-0.6V; DIR at GND; A port=open[4]	-	-	75	uA

Note:

[1] V_{CCI} is the supply voltage associated with the data input port.

[2] V_{CCO} is the supply voltage associated with the output port.

[3] To guarantee the node switches, an external driver must source/sink at least I_{BHLO}/I_{BHHO} when the input is in the range V_{IL} to V_{IH}.

[4] For non bus hold parts only (AiP74LVC8T245).

3.3.4、DC Characteristics 1

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	$V_{CC(B)}$										Unit
			1.5V±0.1V		1.8V±0.15V		2.5V±0.2V		3.3V±0.3V		5.0V±0.5V		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$V_{CC(A)}$=1.5V±0.1V													
propagation delay	t_{PLH}, t_{PHL}	An to Bn	-	17.6	-	15.3	-	13.1	-	12.5	-	12.5	ns
		Bn to An	-	17.5	-	16.3	-	15.2	-	14.4	-	13.8	ns
disable time	t_{PLZ}, t_{PHZ}	$\overline{OE}$ to An	-	29.1	-	29.1	-	29.1	-	29.1	-	29.1	ns
		$\overline{OE}$ to Bn	-	36.4	-	34.5	-	17.3	-	15.5	-	13.6	ns
enable time	t_{PZL}, t_{PZH}	$\overline{OE}$ to An	-	33.6	-	33.6	-	33.6	-	33.6	-	33.6	ns
		$\overline{OE}$ to Bn	-	37.3	-	35.5	-	18.2	-	15.5	-	14.5	ns
$V_{CC(A)}$=1.8V±0.15V													
propagation delay	t_{PLH}, t_{PHL}	An to Bn	-	16.4	-	13.1	-	11.1	-	10.1	-	10.0	ns
		Bn to An	-	15.2	-	12.7	-	11.4	-	10.6	-	10.1	ns
disable time	t_{PLZ}, t_{PHZ}	$\overline{OE}$ to An	-	29.1	-	28.9	-	28.7	-	28.5	-	28.4	ns
		$\overline{OE}$ to Bn	-	36.4	-	32.9	-	15.5	-	14.5	-	13.0	ns
enable time	t_{PZL}, t_{PZH}	$\overline{OE}$ to An	-	24.5	-	24.5	-	24.4	-	24.3	-	24.3	ns
		$\overline{OE}$ to Bn	-	35.5	-	34.5	-	18.2	-	14.2	-	13.5	ns
$V_{CC(A)}$=2.5V±0.2V													
propagation delay	t_{PLH}, t_{PHL}	An to Bn	-	15.3	-	11.9	-	9.2	-	8.2	-	7.6	ns
		Bn to An	-	13.0	-	10.6	-	8.9	-	7.9	-	7.1	ns
disable time	t_{PLZ}, t_{PHZ}	$\overline{OE}$ to An	-	10.9	-	10.9	-	10.9	-	10.9	-	10.9	ns
		$\overline{OE}$ to Bn	-	33.6	-	30.5	-	13.6	-	13.0	-	9.9	ns
enable time	t_{PZL}, t_{PZH}	$\overline{OE}$ to An	-	15.5	-	15.5	-	15.5	-	15.5	-	15.5	ns
		$\overline{OE}$ to Bn	-	33.6	-	29.5	-	15.9	-	12.3	-	10.0	ns
$V_{CC(A)}$=3.3V±0.3V													
propagation delay	t_{PLH}, t_{PHL}	An to Bn	-	14.6	-	11.2	-	8.1	-	7.0	-	6.5	ns
		Bn to An	-	12.3	-	9.8	-	7.9	-	6.8	-	6.0	ns
disable time	t_{PLZ}, t_{PHZ}	$\overline{OE}$ to An	-	10.9	-	10.9	-	10.9	-	10.9	-	10.9	ns
		$\overline{OE}$ to Bn	-	30.9	-	28.2	-	13.2	-	11.4	-	9.5	ns
enable time	t_{PZL}, t_{PZH}	$\overline{OE}$ to An	-	12.3	-	12.3	-	12.1	-	12.0	-	12.0	ns
		$\overline{OE}$ to Bn	-	33.5	-	28.5	-	16.5	-	11.3	-	9.5	ns
$V_{CC(A)}$=5.0V±0.5V													
propagation delay	t_{PLH}, t_{PHL}	An to Bn	-	14.1	-	10.6	-	7.3	-	6.3	-	5.6	ns
		Bn to An	-	12.3	-	9.5	-	7.4	-	6.3	-	5.5	ns
disable time	t_{PLZ}, t_{PHZ}	$\overline{OE}$ to An	-	8.4	-	8.4	-	8.4	-	8.4	-	8.4	ns
		$\overline{OE}$ to Bn	-	32.5	-	29.5	-	12.3	-	10.9	-	8.9	ns
enable time	t_{PZL}, t_{PZH}	$\overline{OE}$ to An	-	9.7	-	9.7	-	9.7	-	9.7	-	9.7	ns
		$\overline{OE}$ to Bn	-	33.5	-	28.5	-	16.7	-	12.3	-	9.7	ns

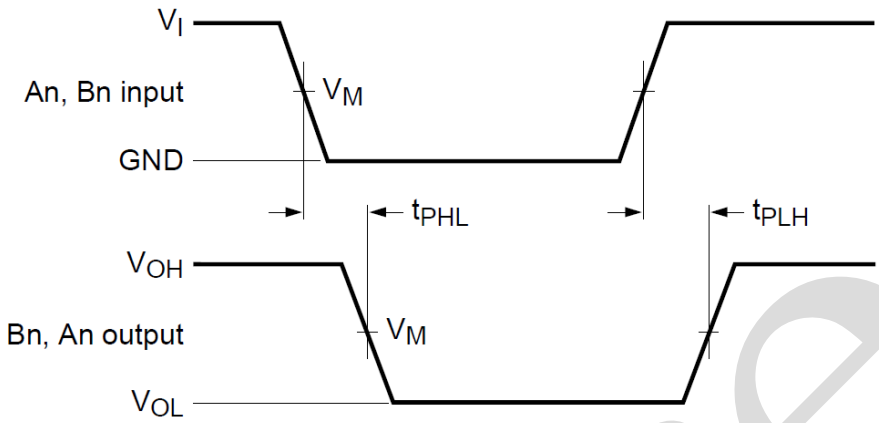
3.3.5、DC Characteristics 2

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	$V_{CC(B)}$										Unit
			1.5V±0.1V		1.8V±0.15V		2.5V±0.2V		3.3V±0.3V		5.0V±0.5V		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$V_{CC(A)}$=1.5V±0.1V													
propagation delay	t_{PLH}, t_{PHL}	An to Bn	-	19.4	-	16.8	-	14.4	-	13.8	-	13.8	ns
		Bn to An	-	19.2	-	17.9	-	16.7	-	15.8	-	15.2	ns
disable time	t_{PLZ}, t_{PHZ}	$\overline{OE}$ to An	-	32	-	32	-	32	-	32	-	32	ns
		$\overline{OE}$ to Bn	-	40	-	38	-	19	-	17	-	15	ns
enable time	t_{PZL}, t_{PZH}	$\overline{OE}$ to An	-	37	-	37	-	37	-	37	-	37	ns
		$\overline{OE}$ to Bn	-	41	-	39	-	20	-	17	-	16	ns
$V_{CC(A)}$=1.8V±0.15V													
propagation delay	t_{PLH}, t_{PHL}	An to Bn	-	18	-	14.4	-	12.2	-	11.1	-	11	ns
		Bn to An	-	16.7	-	14	-	12.5	-	11.7	-	11.1	ns
disable time	t_{PLZ}, t_{PHZ}	$\overline{OE}$ to An	-	32	-	31.8	-	31.6	-	31.3	-	31.2	ns
		$\overline{OE}$ to Bn	-	40	-	36.2	-	17.1	-	16.0	-	14.3	ns
enable time	t_{PZL}, t_{PZH}	$\overline{OE}$ to An	-	27	-	27	-	26.8	-	26.7	-	26.7	ns
		$\overline{OE}$ to Bn	-	39	-	38	-	20	-	15.6	-	14.8	ns
$V_{CC(A)}$=2.5V±0.2V													
propagation delay	t_{PLH}, t_{PHL}	An to Bn	-	16.8	-	13.1	-	10.1	-	9	-	8.4	ns
		Bn to An	-	14.3	-	11.7	-	9.8	-	8.7	-	7.8	ns
disable time	t_{PLZ}, t_{PHZ}	$\overline{OE}$ to An	-	12	-	12	-	12	-	12	-	12	ns
		$\overline{OE}$ to Bn	-	37	-	33.6	-	15	-	14.3	-	10.9	ns
enable time	t_{PZL}, t_{PZH}	$\overline{OE}$ to An	-	17	-	17	-	17	-	17	-	17	ns
		$\overline{OE}$ to Bn	-	37	-	32.5	-	17.5	-	13.5	-	11	ns
$V_{CC(A)}$=3.3V±0.3V													
propagation delay	t_{PLH}, t_{PHL}	An to Bn	-	16.1	-	12.3	-	8.9	-	7.7	-	7.2	ns
		Bn to An	-	13.5	-	10.8	-	8.7	-	7.5	-	6.6	ns
disable time	t_{PLZ}, t_{PHZ}	$\overline{OE}$ to An	-	12	-	12	-	12	-	12	-	12	ns
		$\overline{OE}$ to Bn	-	34	-	31	-	14.5	-	12.5	-	10.4	ns
enable time	t_{PZL}, t_{PZH}	$\overline{OE}$ to An	-	13.5	-	13.5	-	13.3	-	13.2	-	13.2	ns
		$\overline{OE}$ to Bn	-	36.8	-	31.4	-	18.1	-	12.4	-	10.5	ns
$V_{CC(A)}$=5.0V±0.5V													
propagation delay	t_{PLH}, t_{PHL}	An to Bn	-	15.5	-	11.7	-	8	-	6.9	-	6.2	ns
		Bn to An	-	13.5	-	10.5	-	8.1	-	6.9	-	6	ns
disable time	t_{PLZ}, t_{PHZ}	$\overline{OE}$ to An	-	9.2	-	9.2	-	9.2	-	9.2	-	9.2	ns
		$\overline{OE}$ to Bn	-	35.8	-	32.5	-	13.5	-	12	-	9.8	ns
enable time	t_{PZL}, t_{PZH}	$\overline{OE}$ to An	-	10.7	-	10.7	-	10.7	-	10.7	-	10.7	ns
		$\overline{OE}$ to Bn	-	36.8	-	31.4	-	18.4	-	13.5	-	10.7	ns

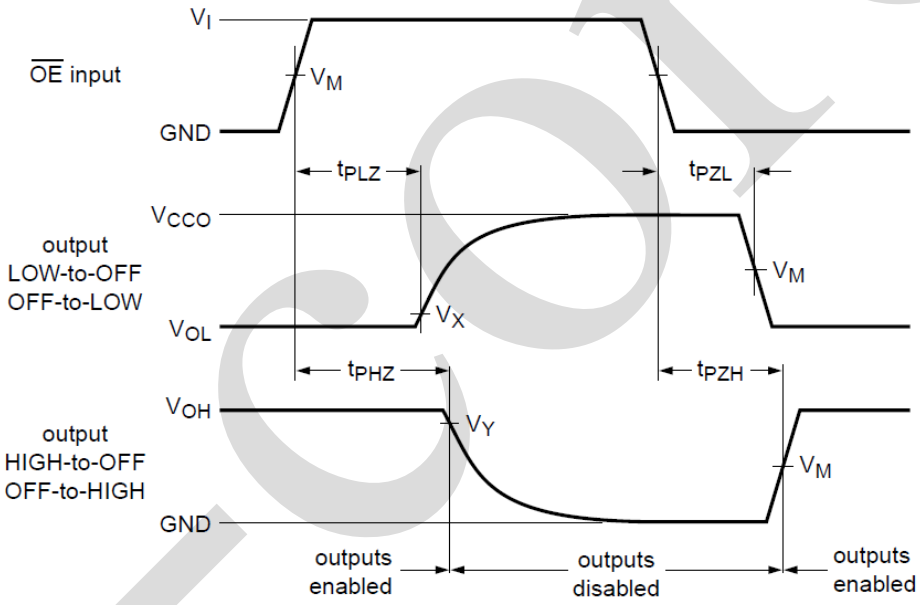
4、Testing Circuit

4.1、AC Testing Waveforms



V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 3. The data input (An, Bn) to output (Bn, An) propagation delay times



V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 4. Enable and disable times

4.2、Measurement Points

Supply voltage	Input[1]	Output[2]		
$V_{CC(A)}$,$V_{CC(B)}$	V_M	V_M	V_X	V_Y
1.2V to 1.6V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL}+0.1V	V_{OH}-0.1V
1.65V to 2.7V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL}+0.15V	V_{OH}-0.15V
3.0V to 5.5V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL}+0.3V	V_{OH}-0.3V

Note:

[1] V_{CCI} is the supply voltage associated with the data input port.

[2] V_{CCO} is the supply voltage associated with the output port.

4.3、AC Testing Circuit

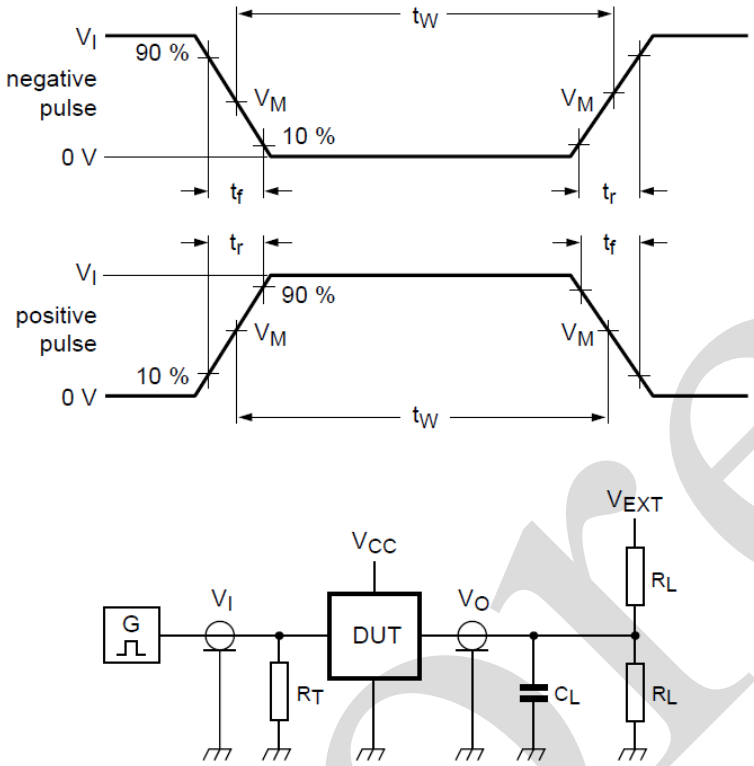


Figure 5. Load circuitry for switching times

Definitions for test circuit:

R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance.

V_{EXT}=External voltage for measuring switching times.

4.4、Test Data

Supply voltage	**Input**		**Load**		**V_{EXT}**		
$V_{CC(A)}$,$V_{CC(B)}$	**V_I[1]**	$\Delta t/\Delta V$[2]	**C_L**	**R_L**	**t_{PLH}, t_{PHL}**	**t_{PZH}, t_{PHZ}**	**t_{PZL}, t_{PLZ}[3]**
1.2V to 5.5V	V_{CCI}	≤1.0ns/V	15pF	2kΩ	open	GND	$2V_{CCO}$

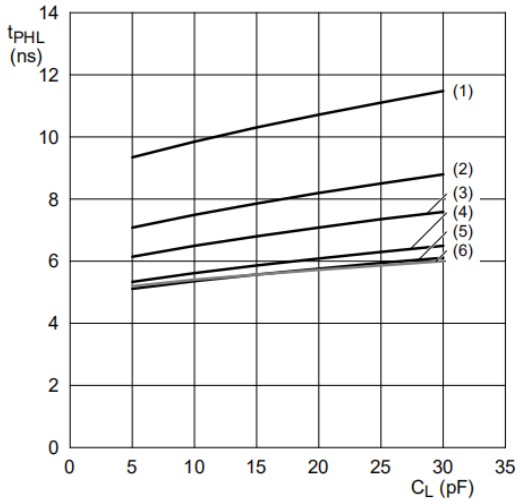
Note:

[1] V_{CCI} is the supply voltage associated with the data input port.

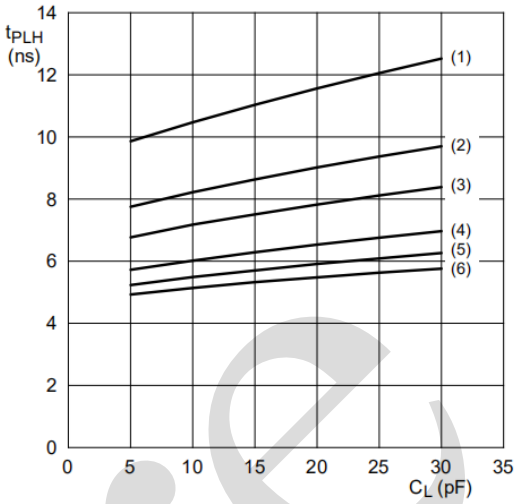
[2] dV/dt≥1.0V/ns.

[3] V_{CCO} is the supply voltage associated with the output port.

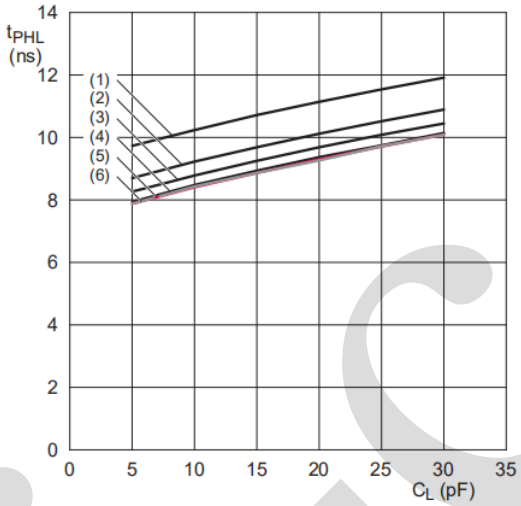
5、Characteristic Curve



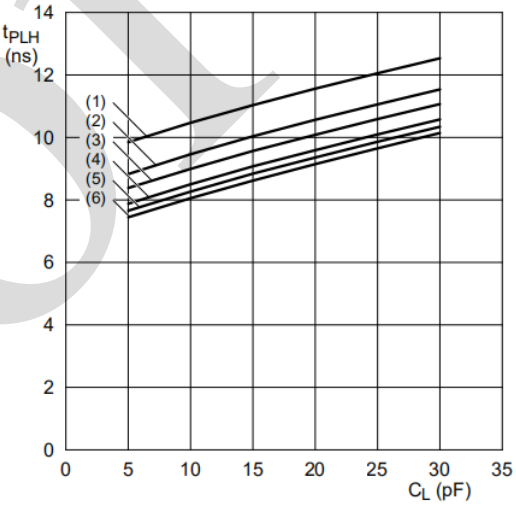
a. HIGH to LOW propagation delay (A to B)



b. LOW to HIGH propagation delay (A to B)



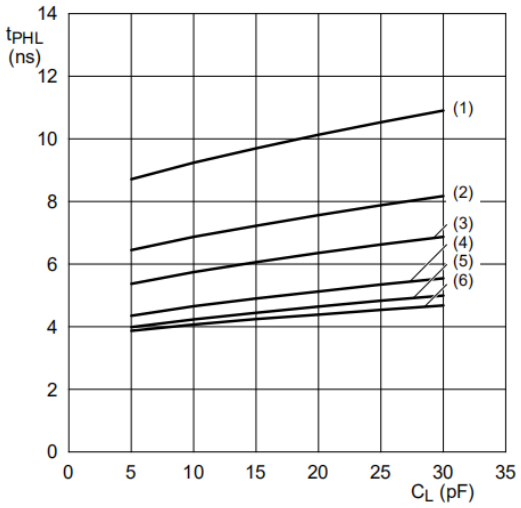
c. HIGH to LOW propagation delay (B to A)



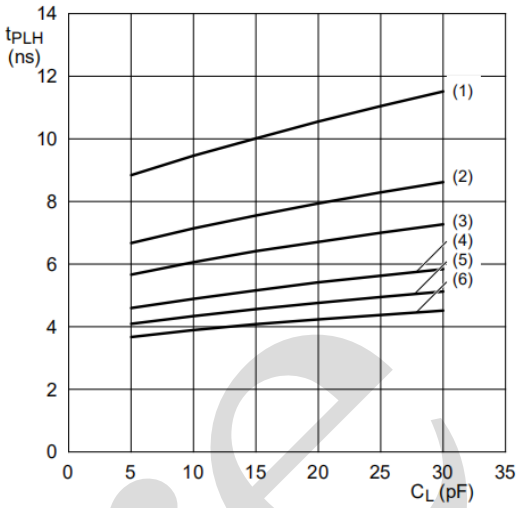
d. LOW to HIGH propagation delay (B to A)

Note: (1) $V_{CC(B)}$=1.2V.
(2) $V_{CC(B)}$=1.5V.
(3) $V_{CC(B)}$=1.8V.
(4) $V_{CC(B)}$=2.5V.
(5) $V_{CC(B)}$=3.3V.
(6) $V_{CC(B)}$=5.0V.

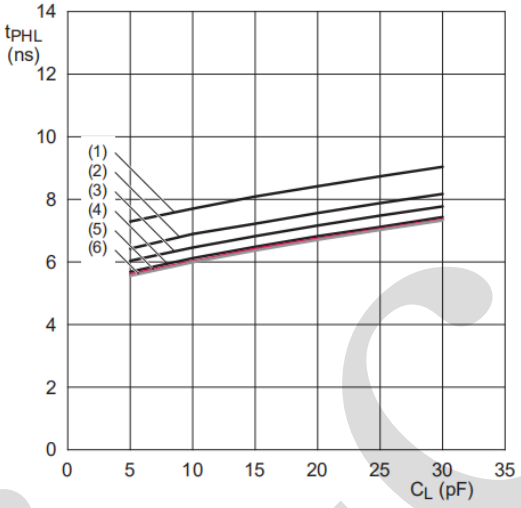
Figure 6. Typical propagation delay versus load capacitance;T_{amb}=25℃;$V_{CC(A)}$=1.2V



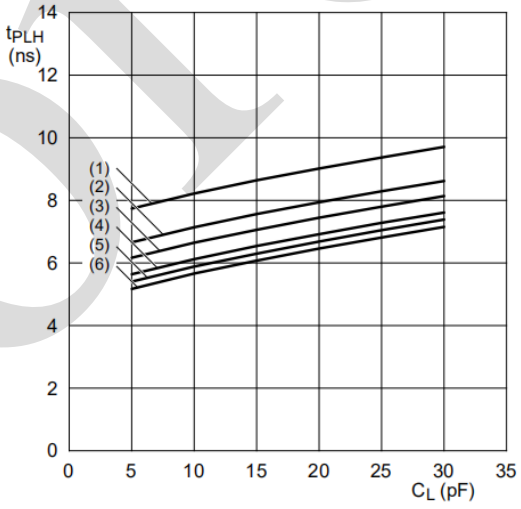
a. HIGH to LOW propagation delay (A to B)



b. LOW to HIGH propagation delay (A to B)



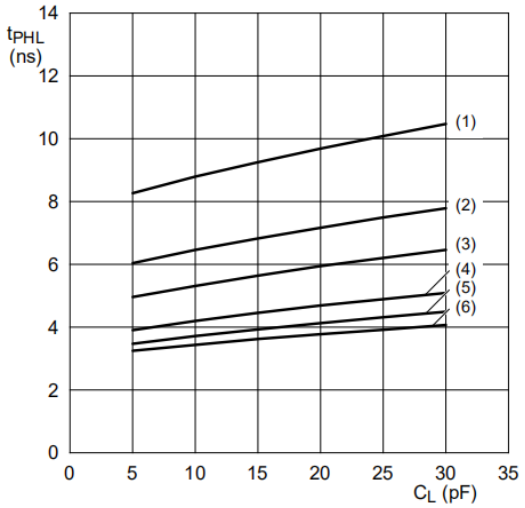
c. HIGH to LOW propagation delay (B to A)



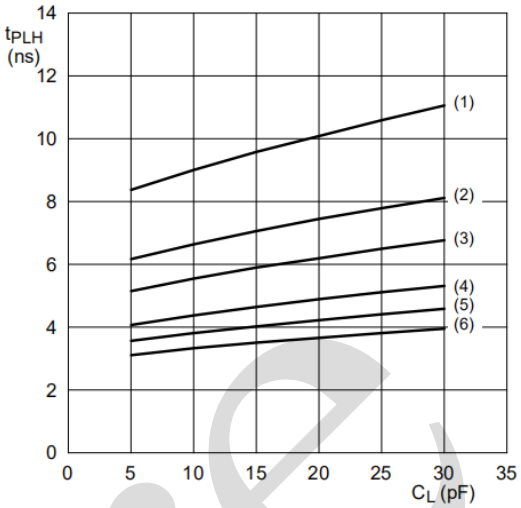
d. LOW to HIGH propagation delay (B to A)

Note: (1) $V_{CC(B)}$=1.2V.
(2) $V_{CC(B)}$=1.5V.
(3) $V_{CC(B)}$=1.8V.
(4) $V_{CC(B)}$=2.5V.
(5) $V_{CC(B)}$=3.3V.
(6) $V_{CC(B)}$=5.0V.

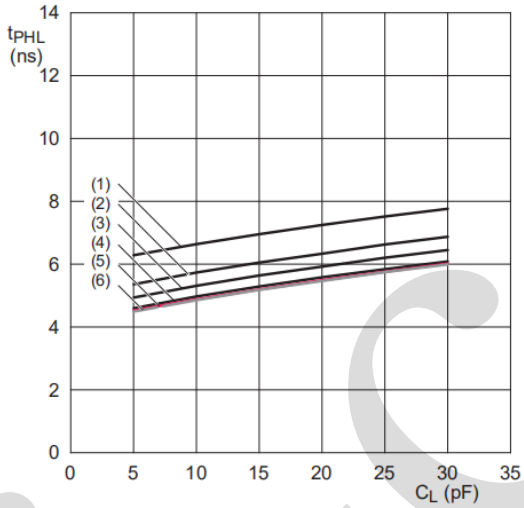
Figure 7. Typical propagation delay versus load capacitance;T_{amb}=25℃;$V_{CC(A)}$=1.5V



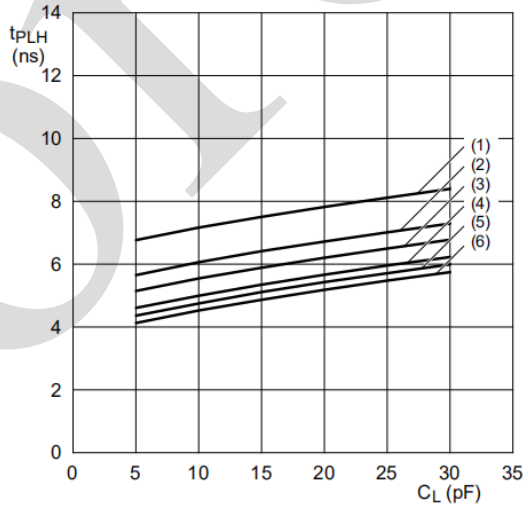
a. HIGH to LOW propagation delay (A to B)



b. LOW to HIGH propagation delay (A to B)



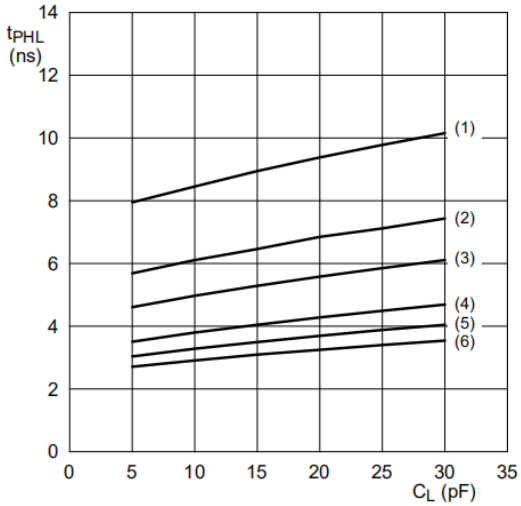
c. HIGH to LOW propagation delay (B to A)



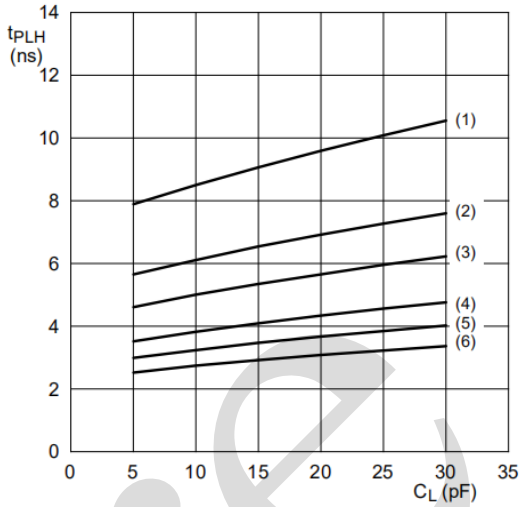
d. LOW to HIGH propagation delay (B to A)

Note: (1) $V_{CC(B)}$=1.2V.
(2) $V_{CC(B)}$=1.5V.
(3) $V_{CC(B)}$=1.8V.
(4) $V_{CC(B)}$=2.5V.
(5) $V_{CC(B)}$=3.3V.
(6) $V_{CC(B)}$=5.0V.

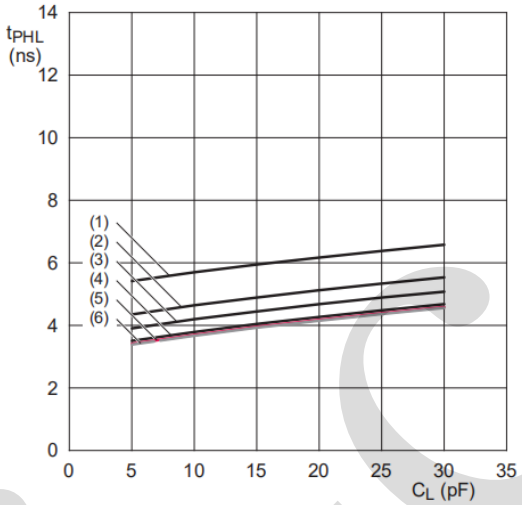
Figure 8. Typical propagation delay versus load capacitance;T_{amb}=25℃;$V_{CC(A)}$=1.8V



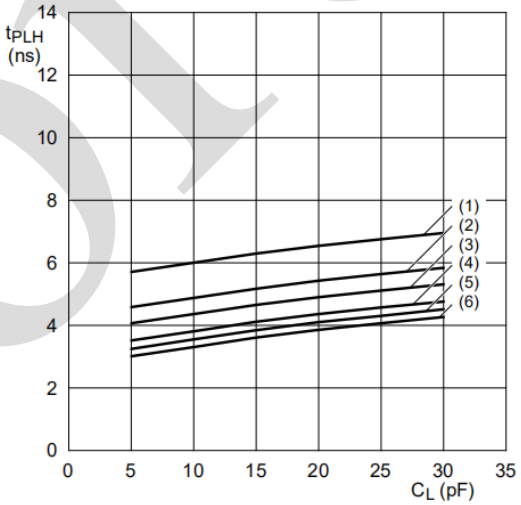
a. HIGH to LOW propagation delay (A to B)



b. LOW to HIGH propagation delay (A to B)



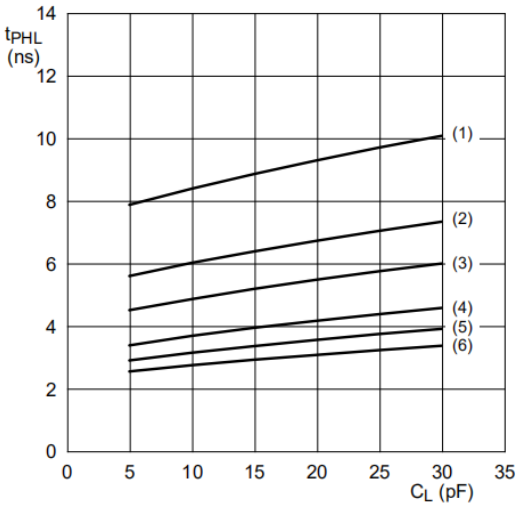
c. HIGH to LOW propagation delay (B to A)



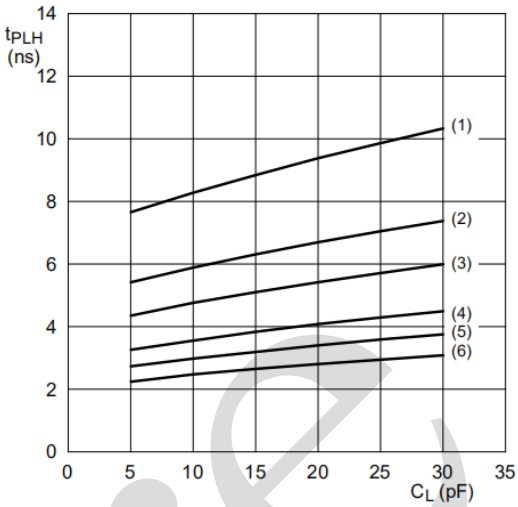
d. LOW to HIGH propagation delay (B to A)

Note: (1) $V_{CC(B)}$=1.2V.
(2) $V_{CC(B)}$=1.5V.
(3) $V_{CC(B)}$=1.8V.
(4) $V_{CC(B)}$=2.5V.
(5) $V_{CC(B)}$=3.3V.
(6) $V_{CC(B)}$=5.0V.

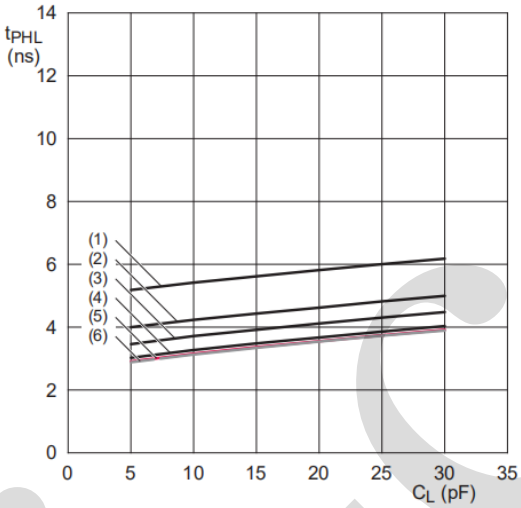
Figure 9. Typical propagation delay versus load capacitance;T_{amb}=25℃;$V_{CC(A)}$=2.5V



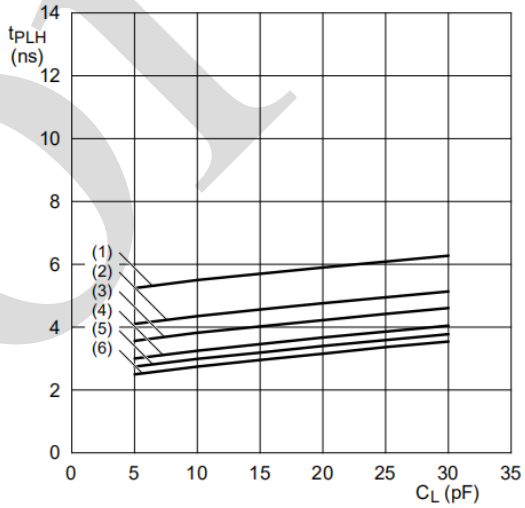
a. HIGH to LOW propagation delay (A to B)



b. LOW to HIGH propagation delay (A to B)



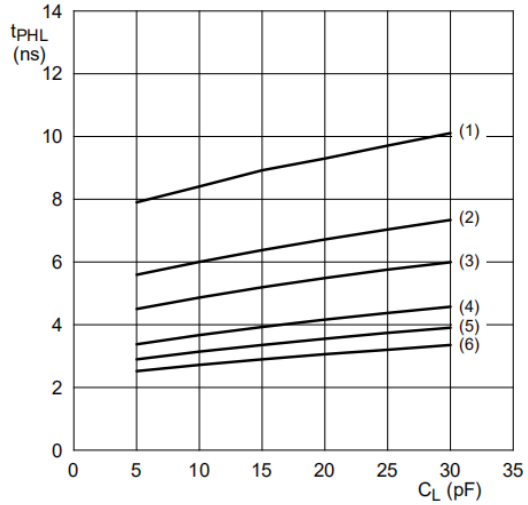
c. HIGH to LOW propagation delay (B to A)



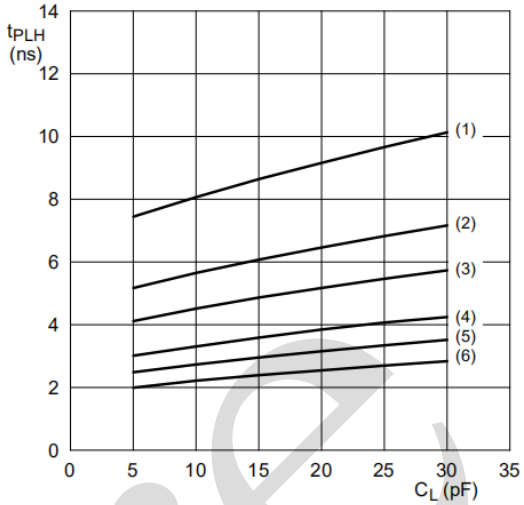
d. LOW to HIGH propagation delay (B to A)

Note: (1) $V_{CC(B)}$=1.2V.
(2) $V_{CC(B)}$=1.5V.
(3) $V_{CC(B)}$=1.8V.
(4) $V_{CC(B)}$=2.5V.
(5) $V_{CC(B)}$=3.3V.
(6) $V_{CC(B)}$=5.0V.

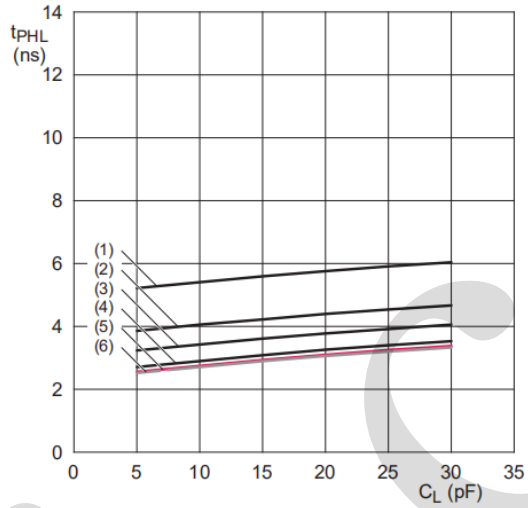
Figure 10. Typical propagation delay versus load capacitance;T_{amb}=25℃;$V_{CC(A)}$=3.3V



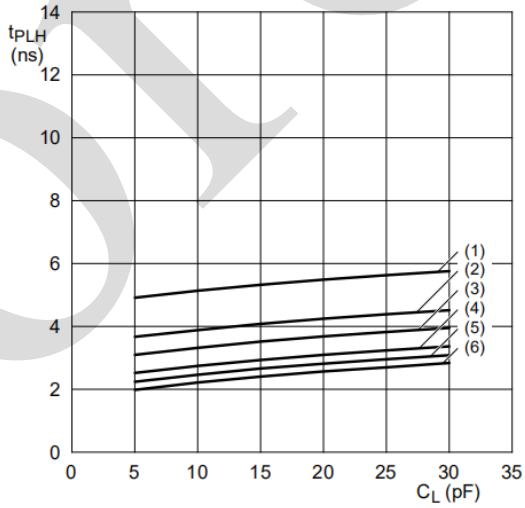
a. HIGH to LOW propagation delay (A to B)



b. LOW to HIGH propagation delay (A to B)



c. HIGH to LOW propagation delay (B to A)



d. LOW to HIGH propagation delay (B to A)

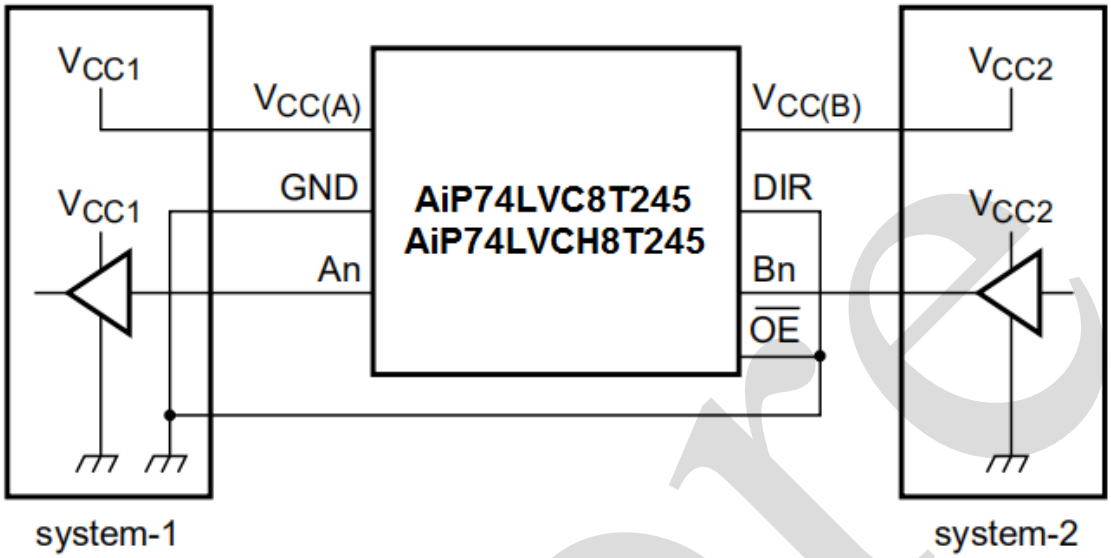
Note: (1) $V_{CC(B)}$=1.2V.
(2) $V_{CC(B)}$=1.5V.
(3) $V_{CC(B)}$=1.8V.
(4) $V_{CC(B)}$=2.5V.
(5) $V_{CC(B)}$=3.3V.
(6) $V_{CC(B)}$=5.0V.

Figure 11. Typical propagation delay versus load capacitance;T_{amb}=25℃;$V_{CC(A)}$=5.0V

6、Typical Application Circuit And Application Note

6.1、Application Circuit 1

The circuit given in Figure 12 is an example of the AiP74LVC8T245; AiP74LVCH8T245 being used in an unidirectional logic level-shifting application.



Schematic given for one channel.

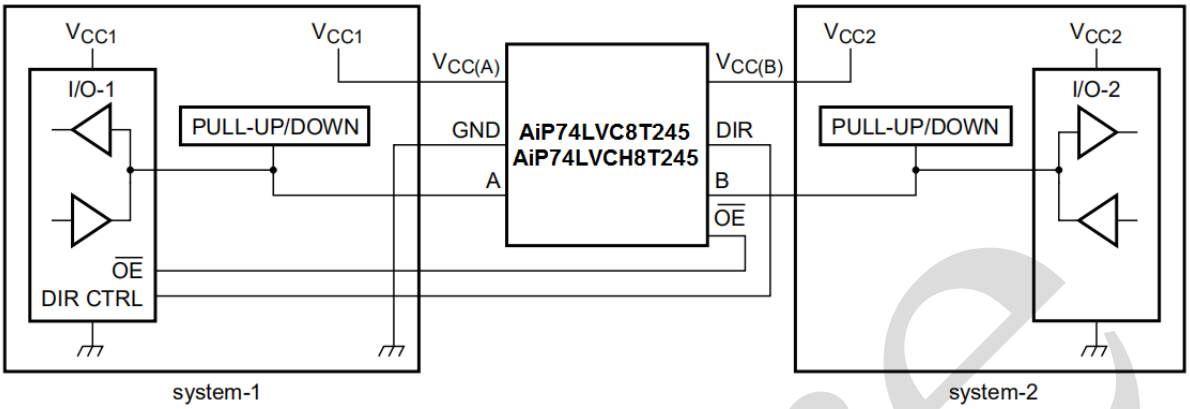
Figure 12. Unidirectional logic level-shifting application

Description unidirectional logic level-shifting application

Name	Function	Description
$V_{CC(A)}$	V_{CC1}	supply voltage of system-1 (1.2V to 5.5V)
GND	GND	device GND
A	OUT	output level depends on VCC1 voltage
B	IN	input threshold value depends on VCC2 voltage
DIR	DIR	the GND (LOW level) determines B port to A port direction
$V_{CC(B)}$	V_{CC2}	supply voltage of system-2 (1.2V to 5.5V)
$\overline{OE}$	$\overline{OE}$	The GND (LOW level) enables the output ports

6.2、Application Circuit 2

Figure 13 shows the AiP74LVC8T245; AiP74LVCH8T245 being used in a bidirectional logic level-shifting application.



Schematic given for one channel.

Pull-up or pull-down only needed for AiP74LVC8T245.

Figure 13. Bidirectional logic level-shifting application

The following table gives a sequence that will illustrate data transmission from system-1 to system-2 and then from system-2 to system-1.

State	DIR CTRL	$\overline{OE}$	I/O-1	I/O-2	Description
1	H	L	output	input	system-1 data to system-2
2	H	H	Z	Z	system-2 is getting ready to send data to system-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on bus hold.
3	L	H	Z	Z	DIR bit is set LOW. I/O-1 and I/O-2 still are disabled. The bus-line state depends on bus hold.
4	L	L	input	output	system-2 data to system-1

Note:H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

6.3、Power-up considerations

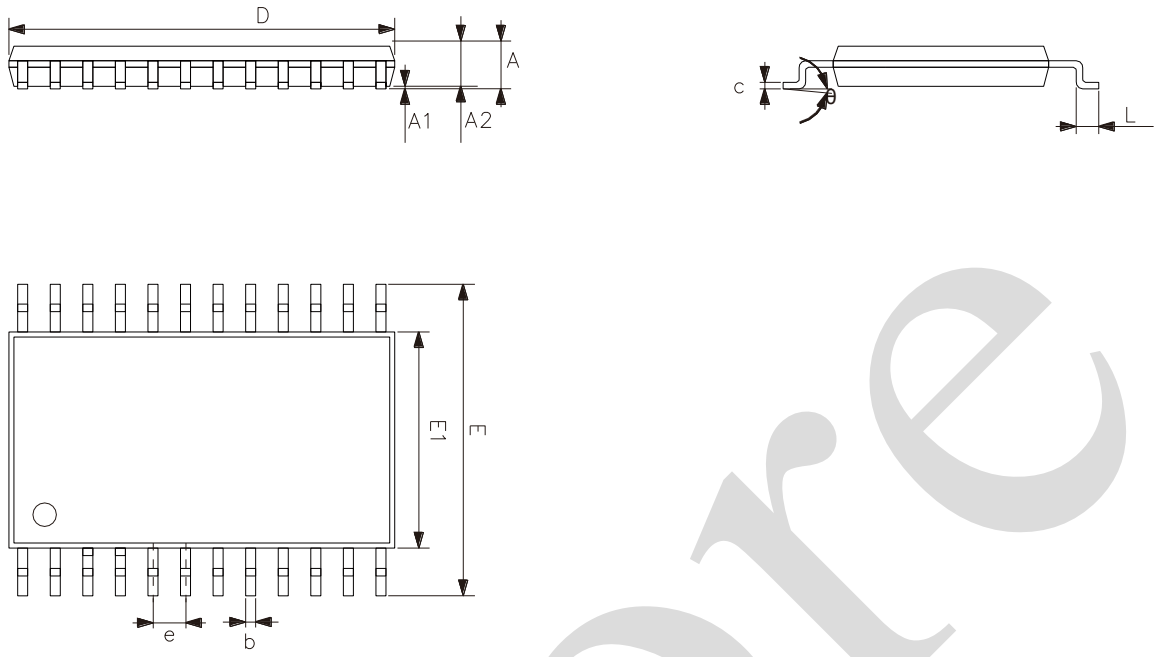
The device is designed such that no special power-up sequence is required other than GND being applied first.

Typical total supply current ($I_{CC(A)}$+$I_{CC(B)}$)

$V_{CC(A)}$	$V_{CC(B)}$					单位
	0V	1.8V	2.5V	3.3V	5.0V	
0V	0	<1	<1	<1	<1	uA
1.8V	<1	<2	<2	<2	2	uA
2.5V	<1	<2	<2	<2	<2	uA
3.3V	<1	<2	<2	<2	<2	uA
5.0V	<1	2	<2	<2	<2	uA

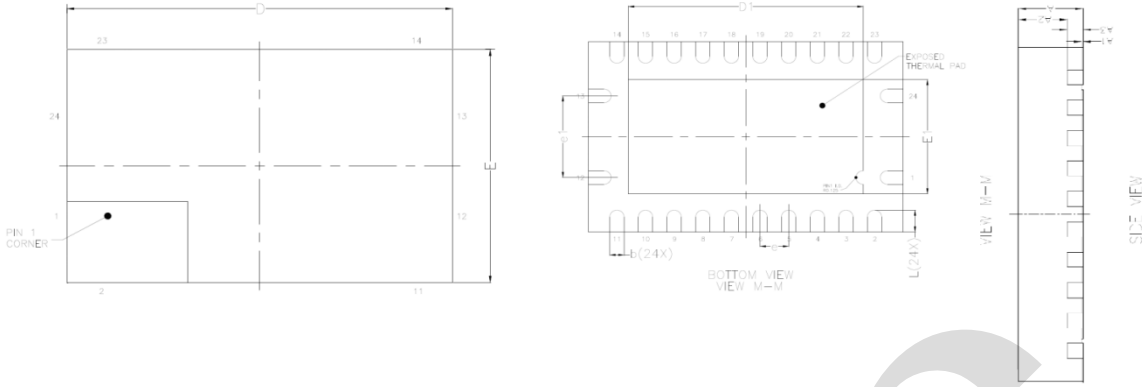
7、Package Information

7.1、TSSOP24



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.20	6.60
E1	4.30	4.50
e	0.65	
L	0.45	0.75
θ	0°	8°

7.2、DHVQFN24



Symbol	Dimensions (mm)	
	Min.	Max.
A	0.80	1.00
A1	0.00	0.05
A2	0.60	0.70
A3	0.20	
D	5.40	5.60
E	3.40	3.60
e	0.50	
e1	1.50	
b	0.18	0.30
L	0.30	0.50
D1	3.95	4.25
E1	1.95	2.25

8、Statements And Notes

8.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

8.2、Notes

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